

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

12.12.01

C. Wills

In re U.S. Patent Application of

HAYASHI et al.

Application Number: To Be Assigned

Filed: Concurrently Herewith

For: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR  
INTEGRATED CIRCUIT

Honorable Assistant Commissioner  
for Patents  
Washington, D.C. 20231

**PRELIMINARY AMENDMENT**

Sir:

Applicant has amended the claims in order to remove multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment. Prior to an examination on the merits, please amend the above-identified application as follows:

**IN THE CLAIMS:**

Please substitute the claims currently on file with the following amended claims:

5. (Amended) A level conversion circuit according to Claim 1, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.
6. (Amended) A level conversion circuit according to Claim 1, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the

00076052-101501

A1